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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,596	12/31/2001	Howard S. David	42390.P13873	2205

8791 7590 10/03/2005

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,11,12 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,11,12 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/28/2005 has been entered.

Response to Amendment

2. This Office action is in response to the Amendment filed on 6/28/2005, claims 9, 11-12, 16-25 are pending in the application.

Claim Objections

3. Claims 9, 20 and 23 are objected to because of the following informalities:

Claims 9, 20 and 23, "a data cache coupled to an eviction buffer, each coupled to the memory device" should be -- a data cache coupled to an eviction buffer, **both** coupled to the memory device-- because it will be better for clarify the connection between the data cache, eviction buffer, and the memory device based on the drawings and description in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Lavelle et al. (US PAT. 6,778,179 hereinafter Lavelle).

Regarding claim 20, Lavelle discloses a system memory (310, figures 6 and 8) comprising at least two memory modules (310a – 310h, figure 8), each memory module including at least one memory device, i.e., DRAM Bank (311, figure 7), and a data cache, i.e., Level 2 cache (312, figure 7) coupled to an eviction buffer, i.e., video buffer/shift register (313, figure 7) is able to configure as parallel-in-serial-out device and output the data sequentially in response to the an external pixel clock (col. 9 line 59 through col. 10 line 2), each coupled to the memory device (figures 7 and 8, col. 8 line 49 through col. 9 line 29, and col. 10 line 57 through col. 11 line 12).

6. Claims 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Kirihata et al. (US PAT. 6,829,682 hereinafter Kirihata).

Regarding claim 20, Kirihata discloses a system memory (300, figure 3) comprising at least two memory modules (DRAM 0 and DRAM 1, figure 4), each memory module including at

least one memory device, i.e., 32 memory cells as defined in figure 4 and (col. 4 lines 40-55), and a data cache, i.e., SDRAM (304, figure 4) with corresponding cells to the memory cells in DRAMs as defined in figure 4 and (col. 4 lines 40-55), coupled to an eviction buffer, i.e., write buffer (314, figure 4), each coupled to the memory device (figures 3-4 and col. 8 line 31 through col. 9 line 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9, 11-12, and 16-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirihata et al. (US PAT. 6,829,682 hereinafter Kirihata) in view of Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 9, Kirihata discloses a system (300, figure 3) comprising a memory controller, i.e., scheduler (306, figure 3) including an array of tag address storage locations (308, figure 3 and col.5 lines 28-38), and a command sequencer and serializer unit, i.e., controller (310, figure 3) coupled to the array of tag address storage locations as defined in figure 3, and system memory couple to the memory module via the address and data buses, system memory including at least two memory modules (302, figure 3), each memory including at least one memory device, i.e., memory cells (302, figure 4), and a data cache, i.e., SDRAM cell (304,

figure 4) and (col. 4 lines 40-55), the data cache coupled to an eviction buffer, i.e., write buffer (314, figure 3), each coupled to the memory device via the address and data buses as defined in figure 3, the data cache controlled by a plurality of commands delivered by the memory controller (figure 4) and (col. 4 lines 56 through col. 5 line 27), although Kirihata does not clearly defined the system is comprising a processor in the drawings, Kirihata discloses the scheduler, i.e., memory controller receives command signal from a controlling entity such as a CPU (col. 4 lines 58-65). Kirihata differs from the claimed invention in not specifically teaches the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a pervious line of data from the data cache into the eviction buffer. However, Akkary teaches in the data cache system comprising a plurality of cache banks (318, figure 2), and a write-back buffer (322, figure 2), both coupled to the system memory (310, figure 2) via the system bus (308, figure 2) to perform memory operation in responds to an instruction from the central processing unit (318, figure 2) via the CPU bus (316, figure 2) and (col. 5 lines 48-59), wherein the write-back buffer is capable to temporary store the eviction entry from the cache bank, and further write back to the main memory, in addition, the cache system of Akkary is further perform a replacement operation in a single clock cycle in which the new cache line is transferred from the filled buffer (320, figure 2), and a victim cache line is simultaneously transferred to write-back buffer for subsequent write-back to main memory (col. 6 lines 11-20, lines 34-67 and figure 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple DRAM array system of Kirihata each comprising a write-back buffer in the same function of cache memory which is used for simultaneous read and write operation (col. 6 lines 12-25),

wherein the memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a pervious line of data from the data cache into the eviction buffer, as per teaching by the data cache system of Akkary, because it eliminates any coherency problems associated with any latency between cache line transfers, and the processing efficiency is enhanced because only a single clock cycles is required to complete both operations (col. 3 lines 55-61).

Regarding claim 11, Akkary discloses the memory controller, i.e., CPU (318, figure 2) to deliver a write back command to the data cache (318, figure 2), the write-back command to cause the previous line of data to be written out of the eviction buffer to the memory device (310, figure 2) and (col. 6 lines 12-20 and line 34 through col. 8 line 27).

Regarding claim 12, discloses the write-back command including way information and bank address information (col. 7 line 48 through col. 8 line 16).

Regarding claim 16, Kirihata discloses a memory controller, i.e., scheduler (306, figure 3), comprising an array of tag address storage location (308, figure 3 and col. 5 lines 28-38), and a command sequencer and serializer unit, i.e., controller (310, figure 3) couple to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache, i.e., SDRAM (304, figures 3-4) and a eviction buffer, i.e., write buffer (314, figures 3-4) with corresponding write buffer cell as defined in figure 4, located on at least one memory module, i.e., DRAM 0 or DRAM 1 (figure 4) of system memory (300, figure 3) and (col. 5 line 28 through col. 6 line 25), the command sequencer and serializer to deliver a write-back command to the eviction buffer associated with the memory module, (col. 4 line 56 through col. 5 line 17, col. 6 lines 49-64, col. 8 line 45 through col. 9 line 2 and figure 5). Kirihata differs from the

claimed invention in not specifically teaches the write-back command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to the memory device. However, Akkary teaches in the data cache system comprising a plurality of cache banks (318, figure 2), and a write-back buffer (322, figure 2), both coupled to the system memory (310, figure 2) via the system bus (308, figure 2) to perform memory operation in responds to an instruction from the central processing unit (318, figure 2) via the CPU bus (316, figure 2) and (col. 5 lines 48-59), wherein the write-back buffer is capable to temporary store the eviction entry from the cache bank, and further write back to the main memory, in addition, the cache system of Akkary is further perform a replacement operation in a single clock cycle in which the new cache line is transferred from the filled buffer (320, figure 2), and a victim cache line is simultaneously transferred to write-back buffer for subsequent write-back to main memory (col. 6 lines 11-20, lines 34-67 and figure 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple DRAM array system of Kirihata each comprising a write-back buffer in the same function of cache memory which is used for simultaneous read and write operation (col. 6 lines 12-25), wherein the write-back command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to the memory device, as per teaching by the data cache system of Akkary, because it eliminates any coherency problems associated with any latency between cache line transfers, and the processing efficiency is enhanced because only a single clock cycles is required to complete both operations (col. 3 lines 55-61).

Regarding claims 17-18, Akkary discloses the memory controller issue an eviction signal to the data cache to evict the previous line of data from the data cache into the eviction buffer,

and also issues the write-back command to cause the previous line of data to be written out of the eviction buffer to the memory device once the memory device is idle (col. 6 lines 12-20 and line 34 through col. 8 line 27).

Regarding claim 19, Akkary discloses the command sequencer and serializer unit, i.e., CPU (318, figure 2) to cause a current line of data to be written from the command sequencer and serialize unit to the data cache (318, figure 2) via the fill buffer (320, figure 2), the command sequencer and serializer unit to cause the previous line of data to be evicted out of the data cache to the eviction buffer, i.e., write-back buffer (322, figure 2) located on the memory module (col. 6 line 12 through col. 8 line 27).

Regarding claim 20, Kirihata discloses a memory module (302, figure 3), comprising at least one memory device, i.e., memory cell in DRAM 0 in figure 4, and a data cache, i.e., SRAM cell (304, figure 4) and (col. 4 lines 40-55) coupled to an eviction buffer, i.e., write buffer cell (314, figure 4), each coupled to the memory device via the address and data buses as defined in figure 3, the data cache controlled by a plurality of commands delivered by a memory controller, i.e., scheduler (306, figure 3), over a memory bus (col. 4 line 56 through col. 5 line 4). Kirihata differs from the claimed invention in not specifically teaches the memory module to receive a write-back command, the write-back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. However, Akkary teaches in the data cache system comprising a plurality of cache banks (318, figure 2), and a write-back buffer (322, figure 2), both coupled to the system memory (310, figure 2) via the system bus (308, figure 2) to perform memory operation in responds to an instruction from the central processing unit (318, figure 2) via the CPU bus (316,

figure 2) and (col. 5 lines 48-59), wherein the write-back buffer is capable to temporary store the eviction entry from the cache bank, and further write back to the main memory, in addition, the cache system of Akkary is further perform a replacement operation in a single clock cycle in which the new cache line is transferred from the filled buffer (320, figure 2), and a victim cache line is simultaneously transferred to write-back buffer for subsequent write-back to main memory (col. 6 lines 11-20, lines 34-67 and figure 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple DRAM array system of Kirihata each comprising a write-back buffer in the same function of cache memory which is used for simultaneous read and write operation (col. 6 lines 12-25), wherein the write-back command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to the memory device, as per teaching by the data cache system of Akkary, because it eliminates any coherency problems associated with any latency between cache line transfers, and the processing efficiency is enhanced because only a single clock cycles is required to complete both operations (col. 3 lines 55-61).

Regarding claim 21, the limitation of the claim are rejected as the same reasons set forth in claim 17.

Regarding claim 22, the limitation of the claim are rejected as the same reasons set forth in claim 12.

Regarding claims 24-25, Kirihata differs from the claimed invention in not specifically teaches a memory module to receive a write-back command, the write-back command to cause a previous line of data, evicted from the data cache, to be written out of the eviction buffer to the memory device of the memory module, and a memory module further to store a current line of

data within a data cache of the memory module, the memory module to evict the previous line of data from the data cache to the eviction buffer located on the memory module in response to a received eviction signal. However, Akkary teaches in the data cache system comprising a plurality of cache banks (318, figure 2), and a write-back buffer (322, figure 2), both coupled to the system memory (310, figure 2) via the system bus (308, figure 2) to perform memory operation in responds to an instruction from the central processing unit (318, figure 2) via the CPU bus (316, figure 2) and (col. 5 lines 48-59), wherein the write-back buffer is capable to temporary store the eviction entry from the cache bank, and further write back to the main memory, in addition, the cache system of Akkary is further perform a replacement operation in a single clock cycle in which the new cache line is transferred from the filled buffer (320, figure 2), and a victim cache line is simultaneously transferred to write-back buffer for subsequent write-back to main memory (col. 6 lines 11-20, lines 34-67 and figure 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module (302, figure 3) of Kirihata is able to receive a write-back command, the write-back command to cause a previous line of data, evicted from the data cache, to be written out of the eviction buffer to the memory device of the memory module, and a memory module further to store a current line of data within a data cache of the memory module, the memory module to evict the previous line of data from the data cache to the eviction buffer located on the memory module in response to a received eviction signal, as per teaching by the computer system of Akkary, because it eliminates any coherency problems associated with any latency between cache line transfers, and the processing efficiency is enhanced because only a single clock cycles is required to complete both operations (col. 3 lines 55-61).

Response to Arguments

9. Applicant's arguments with respect to claims 9, 11-12 and 16-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kershaw (US PAT. 6,490,655) discloses data processing apparatus and method for cache line replacement responsive to the operational state of memory (abstract).

Parks (US PAT. 6,356,983) discloses system and method providing cache coherency and atomic memory operations in a multiprocessor computer architecture (abstract).

Quach (US PAT. 5,659,709) discloses write-back and snoop write-back buffer to prevent deadlock and to enhance performance in an in-order protocol multiprocessing bus (col. 3 line 49 through col. 5 line 58).

Kronstadt et al. (US PAT. 4,725,945) discloses distributed cache in dynamic RAMs wherein the system memory comprising a plurality of banks (16), each bank consists of an array of DRAMs and on-chip data cache (24) as show in figure 3 and (col. 2 lines 3-28).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2189

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PRIMARY EXAMINER